IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kalpesh Mehta et al.	Art Unit:	2628
Serial No.:	10/759,504	Examiner:	Joni Hsu
Filed:	January 16, 2004	Assignee:	Intel Corporation
Title:	CALCULATING DISPLAY MODE VALUES		

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BRIEF ON APPEAL

This Brief on Appeal perfects the Notice of Appeal filed May 7, 2007.

(1) Real Party in Interest

This case is assigned of record to Intel Corporation, who is the real party in interest.

(2) Related Appeals and Interferences

There are no known related appeals and/or interferences.

(3) Status of Claims

Claims 1-25 and 30-38 are pending and under consideration.

Claims 26-29 have been canceled.

Claims 1-25 and 30-38 stand rejected.

Claims 1, 12, 22, and 36 are in independent form.

Claims 1-25 and 30-38 are involved in the appeal, either directly or by virtue of depending from one of independent claims 1, 12, 22, and 36.

(4) Status of Amendments

A response after final rejection was filed under 37 C.F.R. § 1.116 on April 9, 2007. No claim amendments were set forth in the April 9 response.

An advisory action mailed April 17, 2007 did not indicate whether the proposed amendment(s) would be entered for purposes of appeal. However, in light of the fact that no claim amendments were set forth in the April 9 response, the appeal can proceed without regard to entry of the April 9 response.

(5) Summary of Claimed Subject Matter

Claim 1 relates to a method of determining buffer management information for a data processing system. The method includes:

determining a latency parameter based on a first system configuration of the data processing system, the latency parameter representing a latency time amount between a display data request and delivery of display data to a display buffer (*id.*, page 6, line 1-4);

determining a buffer drain rate based on a first display mode of the data processing system (*id.*, page 6, line 6-10);

calculating one or more buffer management parameters based on at least the latency parameter and the buffer drain rate(*id.*, page 2, line 21-page 3, line 1; page 3, line 21-page 4, line 3; page 4, line 12-22; page 6, line 21-page 9, line 2; page 11, line 6 - page 12, line 15); and

making the one or more buffer management parameters available for management of the display buffer. *Id.*, page 3, line 6-11; page 4, line 3-9; page 12, line 16-18.

Claim 15 relates to an apparatus that includes

a display part which directs movement of display data (*id.*, page 4, line 3-5), the display part including a buffer to store display data to be displayed on a display screen (*id.*, page 4, line 5-11); and

a data computing system configured to calculate one or more buffer management parameters based on a latency parameter based on a first system configuration and a buffer drain rate based on a first display mode (*id.*, page 2, line 21-page 3, line 11);

wherein the latency parameter represents a latency time amount between a display data request and delivery of display data to the buffer (*id.*, page 6, line 1-4); and

wherein the buffer drain rate represents a rate at which the display data is read from the buffer. *Id.*, page 6, line 6-10.

Claim 29 relates to an article that includes a storage medium which stores computer-executable instructions. The instructions are readable and operable to cause a computer to perform operations. *Id.*, page 3, line 21-page 4, line 3. The operations include:

determining a latency parameter based on a first system configuration of the data processing system, the latency parameter representing a latency time amount between a display data request and delivery of display data to a display buffer (*id.*, page 6, line 1-4);

determining a buffer drain rate based on a first display mode (*id.*, page 6, line 6-10);

calculating one or more buffer management parameters based on at least the latency parameter and the buffer drain rate (*id.*, page 2, line 21-page 3, line 1; page 3, line 21-page 4, line 3; page 4, line 12-22; page 6, line 21-page 9, line 2; page 11, line 6 - page 12, line 15); and

making the one or more buffer management parameters available for management of the display buffer. *Id.*, page 3, line 6-11; page 4, line 3-9; page 12, line 16-18.

Claim 43 relates to a system that includes:

a display (*id.*, page 3, line 16-20);

a display part which directs movement of display data to the display (*id.*, page 4, line 3-5), the display part including a buffer to store display data to be displayed on the display (*id.*, page 4, line 5-11); and

a data processor configured to calculate one or more buffer management parameters based on a latency parameter based on a first system configuration and a buffer drain rate based on a first display mode (*id.*, page 2, line 21-page 3, line 11);

wherein the latency parameter represents a latency time amount between a display data request and delivery of display data to the buffer (*id.*, page 6, line 1-4); and

wherein the buffer drain rate represents a rate at which the display data is read from the buffer. *Id.*, page 6, line 6-10.

Claim 57 relates to a method of determining buffer management information for a data processing system. The method includes:

determining a maximum amount of time that access to a local memory to obtain data to supply a display FIFO buffer memory may be delayed (*id.*, page 6, line 1-4);

determining a drain rate at which data is to be drained from the display FIFO buffer memory based on a display mode supported by a graphics processor (*id.*, page 6, line 6-10);

calculating a watermark value based on at least the maximum amount of time and the drain rate (*id.*, page 2, line 21-page 3, line 1; page 3, line 21-page 4, line 3; page 4, line 12-22; page 6, line 21-page 7, line 10; page 8, line 14-page 9, line 2; page 11, line 6 - page 12, line 15); and

making the watermark value available for management of the display FIFO buffer memory. *Id.*, page 3, line 6-11; page 4, line 3-9; page 12, line 16-18.

Claim 60 relates to a method of determining buffer management information for a data processing system. The method includes:

determining a maximum amount of time that access to a local memory to obtain data to supply a display FIFO buffer memory may be delayed (*id.*, page 6, line 1-4);;

determining a drain rate at which data is to be drained from the display FIFO buffer memory based on a display mode supported by a graphics processor (*id.*, page 6, line 6-10);

calculating a burst length value based on at least the maximum amount of time and the drain rate (*id.*, page 2, line 21-page 3, line 1; page 3, line 21-page 4, line 3; page 4, line 12-22; page 7, line 11-page 8, line 13; page 11, line 6 - page 12, line 15); and

making the burst length value available for management of the display FIFO buffer memory. *Id.*, page 3, line 6-11; page 4, line 3-9; page 12, line 16-18.

(6) Grounds of Rejection to be Reviewed on Appeal

As set forth in the following concise statements, the following grounds for rejection are presented for review on appeal:

Ground 1: whether claims 1-14, 29-42, and 57-62 are properly rejected under 35 U.S.C. § 101 as directed to non-statutory subject matter; and

Ground 2: whether claims 1-6, 10-20, 24-34, 38-48, and 52-57 are properly rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,953,020 to Wang et al. (hereinafter "Wang") and U.S. Patent No. 6,499,072 to Frank et al. (hereinafter "Frank").

(7) Argument

The organization of the arguments presented hereinafter follows the organization of the grounds for rejection to reviewed on appeal set forth above. In particular, separate boldfaced headings for the grounds presented for review follow.

Ground 1: Rejections under 35 U.S.C. § 101

Claim 1 was rejected under 35 U.S.C. § 101 as allegedly being directed to a judicial exception to statutory subject matter defined in 35 U.S.C. § 101. In particular, the rejection of claim 1 contends that making useful parameters available is not a tangible result because it is not clear whether the parameters will "actually be used" for a described utility.

Applicant respectfully disagrees. Intermediates have long been recognized as deriving their utility from a *potential* use in generating final products of known utility. *See, e.g., M.P.E.P.* § 2107.01 (describing that intermediates lack a utility only when a final product has no utility). In claim 1, since the final product of management of the display buffer has a specific, substantial, and credible utility, the making of buffer management parameters suitable for management of the display buffer available also has utility.

The Advisory action mailed April 17, 2007 contends that the production of an intermediate for generating a product of known utility is not a "tangible result" or a "practical application" unless the claim recites that the intermediate "will actually be used" in generating the product of known utility. Applicant respectfully disagrees and submits that it is self-evident that intermediates can derive their utility from a potential use in generating final products of known utility. Indeed, no court known to the undersigned has ever identified a failure to recite "actual use" as establishing a judicial exception to the statutory subject matter defined in 35 U.S.C. § 101.

Accordingly, the rejection of claim 1 under 35 U.S.C. § 101 is improper and applicant asks that it be withdrawn.

Claim 29 was rejected under 35 U.S.C. § 101 as allegedly being directed to a judicial exception to the statutory subject matter defined in 35 U.S.C. § 101. In particular, the rejection of claim 29 appears to contend that an "article comprising a storage medium" is not patentable subject matter but a "computer program product that comprises a computer readable medium" is patentable subject matter. The alleged basis for this distinction is that an article "could be taken to be an entity that is completely separate from a computer and simply stores the instructions without the computer reading the instruction[s] and executing those instructions."

Applicant respectfully disagrees with the rejection on several bases. To begin with, 35 U.S.C. § 101 does not preclude entities that are "completely separate from a computer" from patentability. Indeed, much of 35 U.S.C. § 101 was written before the invention of many computers. It would border on the absurd for the legislature to have drafted a law precluding articles from patentability if they were "completely separate" from devices that had not yet been invented.

Moreover, there is no basis for the contention that articles which store instructions without a computer reading the instructions are not patentable subject matter. For example, M.P.E.P. § 2106.01 states that:

> "a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. *See M.P.E.P.* § 2106.01 (*citing In re Lowry*, 32 F.3d 1579, 1583-84 (Fed. Cir. 1994).

Note that there is no requirement that a computer read a computer program encoded on a computer-readable medium set forth in the M.P.E.P. Instead, a computer-readable medium encoded with a computer program defines structural and functional interrelationships and hence constitutes patentable subject matter. Since claim 29 recites "an article [that comprises] a storage medium which stores computer-executable instructions, the instructions being readable and operable to cause a computer to perform operations," claim 29 is statutory.

Accordingly, the rejection of claim 29 under 35 U.S.C. § 101 is improper and applicant asks that it be withdrawn.

Ground 2: Rejections under 35 U.S.C. § 103(a) as obvious over Wang and Frank

Claims 1 and 29 were rejected under 35 U.S.C. § 103(a) as obvious over Wang and Frank.

The rejections of claims 1 and 29 are based on the contention that Frank's data issue delay data 24 constitutes a latency parameter. In particular, the rejections contend that "the latency time amount between a display data request and delivery of display data to a display buffer is essentially the amount of time it takes for the display engine to access the memory to obtain display data."

This is simply not true. Indeed, Frank himself provides support for the opposite conclusion. In this regard, Frank's data issue delay data 24 indicates the delay that a sequencer needs to provide for adjusting the issuance of data read commands over regulated channels from the frame buffer to allow data from the unregulated bus to be transferred over a memory read backbone. *See Frank*, col. 4, line 32-35.

In other words, Frank's data issue delay data 24 represents an artificial delay imposed before the issuance of a data read command. Applicant respectfully submits that it is not reasonable to consider a delay before the issuance of a read command to constitute a time between issuance of a display data

request and delivery of display data. Indeed, Frank himself acknowledges this distinction. *See, e.g., Frank*, col. 2, line 54-56 (describing that an "adjustable delay sequencer selectively throttles data reads from the frame buffer memory so that data collisions do not occur over the memory read backbone"); col. 2, line 59-63 (describing that the rate at which data is obtained from the frame buffer is regulated by adjusting "the amount of delay between consecutive memory reads").

Since Frank's data issue delay is imposed to throttle consecutive memory reads, the amount of time Frank requires for a display engine to access a memory to obtain display data is this artificially imposed data issue delay. The data issue delay is not "essentially" the latency time amount between a display data request and delivery of display data. It is a different parameter intentionally imposed by Frank because unregulated operation was insufficient.

The Advisory action mailed April 17, 2007 contends that the claims do "not recite that the latency parameter cannot be an artificial delay imposed on the issuance of a data read command." Applicant respectfully disagrees. In this regard, a

delay before the issuance of a data read command is clearly prior to the issuance of a data read command, rather than "between a display data request and delivery of display data to a display buffer," as recited in claims 1 and 29.

Wang does nothing to remedy these deficiencies in Frank. As discussed in the response filed November 28, 2006, Wang was clearly aware of latency between the memory controller accepting a request and data return. *See, e.g., Wang*, col. 2, line 36-39. However, nothing in Wang describes or suggests that parameters characterizing this latency should be determined and calculations based thereon. Any contention that it would have been obvious for one of ordinary skill to have done so represents hindsight-based reconstruction of Applicant's technology using Applicant's disclosure as a guide.

Accordingly, claims 1 and 29 are not obvious over Wang and Frank. Applicant therefore requests that the rejections of claims 1, 29, and the claims dependent therefrom be withdrawn.

Claim 15 was rejected under 35 U.S.C. § 103(a) as obvious over Wang and Frank.

The rejection of claim 15 is based on the contention that Frank's data issue delay data 24 constitutes a latency parameter. Applicant respectfully disagrees and instead contends that even if Wang and Frank were combined as suggested, one of ordinary skill would not arrive at the claimed subject matter.

Like claims 1 and 29, claim 15 also explicitly recites that a "latency parameter represents a latency time amount between a display data request and delivery of display data to the buffer." As discussed above, Frank's data issue delay data 24 is prior to the issuance of a data read command, not between a display data request and delivery and is thus not a latency parameter as recited.

Accordingly, claim 15 is not obvious over Wang and Frank. Applicant therefore requests that the rejections of claim 15 and the claims dependent therefrom be withdrawn.

Claim 43 was rejected under 35 U.S.C. § 103(a) as obvious over Wang and Frank.

Like claims 1, 15, and 29, claim 43 also explicitly recites that a "latency parameter represents a latency time amount

between a display data request and delivery of display data to the buffer." As discussed above, Frank's data issue delay data 24 is not the time between a display data request and delivery and is thus not a latency parameter as recited.

Accordingly, claim 43 is not obvious over Wang and Frank. Applicant therefore requests that the rejections of claim 43 and the claims dependent therefrom be withdrawn.

Claim 57 was rejected under 35 U.S.C. § 103(a) as obvious over Wang and Frank.

Wang and Frank neither describe nor suggest elements and/or limitations recited in claim 57. For example, Wang and Frank neither describe nor suggest that a maximum amount of time that access to a local memory to obtain data to supply a display FIFO buffer memory may be delayed is determined. As discussed above, Frank's data issue delay data 24 is an artificially imposed delay prior to the issuance of a data read command.

Even if one of ordinary skill were to take this time prior to the issuance of a data read command to be between a display data request and delivery (which applicant does not concede), claim 57 is still not obvious over Wang and Frank. In this regard, claim 57 recites a maximum amount of time that access to a local memory to obtain data to supply a display FIFO buffer memory may be delayed. Such a maximum amount of time clearly

includes the sum of Frank's data issue delay data and any latency time between a display data request and delivery of display data.

Accordingly, claim 57 is not obvious over Wang and Frank. Applicant therefore requests that the rejection of claim 57 be withdrawn.

Please apply the $500 brief fee and any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: July 9, 2007

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Appendix of Claims

1. A method of determining buffer management information for a data processing system, comprising:

determining a latency parameter based on a first system configuration of the data processing system, the latency parameter representing a latency time amount between a display data request and delivery of display data to a display buffer;

determining a buffer drain rate based on a first display mode of the data processing system;

calculating one or more buffer management parameters based on at least the latency parameter and the buffer drain rate; and

making the one or more buffer management parameters available for management of the display buffer.

2. The method of claim 1, further comprising:

determining a buffer fill rate based on a buffer configuration; and

calculating at least one of the one or more buffer management parameters based on the buffer fill rate.

3. The method of claim 1, further comprising:

calculating at least one of the one or more buffer management parameters based on a buffer size.

4. The method of claim 1, wherein the one or more buffer management parameters comprise a watermark level.

5. The method of claim 4, wherein the watermark level comprises a lower bound of a desired watermark level range.

6. The method of claim 4, wherein the watermark level comprises an upper bound of a desired watermark level range.

7. The method of claim 1, wherein the one or more buffer management parameters comprise a burst length.

8. The method of claim 7, wherein the burst length comprises a lower bound of a desired burst length range.

9. The method of claim 7, wherein the burst length comprises an upper bound of a desired burst length range.

10. The method of claim 1, further comprising:

detecting a change from the first display mode to a second display mode; and

calculating at least one of the one or more buffer management parameters based on the second display mode.

11. The method of claim 1, further comprising:

detecting a change from the first system configuration to a second system configuration; and

calculating at least one of the one or more buffer management parameters based on the second system configuration.

12. The method of claim 1, wherein the latency parameter represents a maximum expected latency time amount for the first system configuration of the data processing system.

13. The method of claim 1, wherein the first display mode is characterized by at least one of a first refresh rate, a first display resolution, and a first color depth.

14. The method of claim 1, wherein the first system configuration is characterized at least by a buffer memory type.

15. An apparatus comprising:

a display part which directs movement of display data, the display part including a buffer to store display data to be displayed on a display screen; and

a data computing system configured to calculate one or more buffer management parameters based on a latency parameter based on a first system configuration and a buffer drain rate based on a first display mode;

wherein the latency parameter represents a latency time amount between a display data request and delivery of display data to the buffer; and

wherein the buffer drain rate represents a rate at which the display data is read from the buffer.

16. The apparatus of claim 15, wherein the data computing system is further configured to calculate at least one of the one or more buffer management parameters based on a buffer fill rate, the buffer fill rate based on a configuration of the buffer.

17. The apparatus of claim 15, wherein the data computing system is further configured to calculate at least one of the one or more buffer management parameters based on a buffer size.

18. The apparatus of claim 15, wherein the one or more buffer management parameters comprise a watermark level.

19. The apparatus of claim 18, wherein the watermark level comprises a lower bound of a desired watermark level range.

20. The apparatus of claim 18, wherein the watermark level comprises an upper bound of a desired watermark level range.

21. The apparatus of claim 15, wherein the one or more buffer management parameters comprise a burst length.

22. The apparatus of claim 21, wherein the burst length comprises a lower bound of a desired burst length range.

23. The apparatus of claim 21, wherein the burst length comprises an upper bound of a desired burst length range.

24. The apparatus of claim 15, wherein the data computing system is further configured to detect a change from a first display mode to a second display mode, and in response to the detecting is further configured to calculate at least one of the one or more buffer management parameters based on the second display mode.

25. The apparatus of claim 15, wherein the data computing system is further configured to detect a change from a first system configuration to a second system configuration, and in response to the detecting is further configured to calculate at least one of the one or more buffer management parameters based on the second system configuration.

26. The apparatus of claim 15, wherein the latency parameter represents a maximum expected latency time amount for the first system configuration.

27. The apparatus of claim 15, wherein the first display mode is characterized by at least one of a first refresh rate, a first display resolution, and a first color depth.

28. The apparatus of claim 15, wherein the first system configuration is characterized at least by a first buffer memory type.

29. An article comprising a storage medium which stores computer-executable instructions, the instructions being readable and operable to cause a computer to perform operations comprising:

determining a latency parameter based on a first system configuration of the data processing system, the latency parameter representing a latency time amount between a display data request and delivery of display data to a display buffer;

determining a buffer drain rate based on a first display mode;

calculating one or more buffer management parameters based on at least the latency parameter and the buffer drain rate; and

making the one or more buffer management parameters available for management of the display buffer.

30. The article of claim 29, the operations further comprising:

determining a buffer fill rate based on a buffer configuration; and

calculating at least one of the one or more buffer management parameters based on the buffer fill rate.

31. The article of claim 29, the operations further comprising:

calculating at least one of the one or more buffer management parameters based on a buffer size.

32. The article of claim 29, wherein the one or more buffer management parameters comprise a watermark level.

33. The article of claim 32, wherein the watermark level comprises a lower bound of a desired watermark level range.

34. The article of claim 32, wherein the watermark level comprises an upper bound of a desired watermark level range.

35. The article of claim 29, wherein the one or more buffer management parameters comprise a burst length.

36. The article of claim 35, wherein the burst length comprises a lower bound of a desired burst length range.

37. The article of claim 35, wherein the burst length comprises an upper bound of a desired burst length range.

38. The article of claim 29, the operations further comprising:

detecting a change from the first display mode to a second display mode; and

calculating at least one of the one or more buffer management parameters based on the second display mode.

39. The article of claim 29, the operations further comprising:

detecting a change from the first system configuration to a second system configuration; and

calculating at least one of the one or more buffer management parameters based on the second system configuration.

40. The article of claim 29, wherein the latency parameter represents a maximum expected latency time amount for the first system configuration of the data processing system.

41. The article of claim 29, wherein the first display mode is characterized by at least one of a first refresh rate, a first display resolution, and a first color depth.

42. The article of claim 29, wherein the first system configuration is characterized at least by a buffer memory type.

43. A system comprising:

a display;

a display part which directs movement of display data to the display, the display part including a buffer to store display data to be displayed on the display; and

a data processor configured to calculate one or more buffer management parameters based on a latency parameter based on a first system configuration and a buffer drain rate based on a first display mode;

wherein the latency parameter represents a latency time amount between a display data request and delivery of display data to the buffer; and

wherein the buffer drain rate represents a rate at which the display data is read from the buffer.

44. The system of claim 43, wherein the data processor is further configured to calculate at least one of the one or more buffer management parameters based on a buffer fill rate, the buffer fill rate based on a configuration of the buffer.

45. The system of claim 43, wherein the data processor is further configured to calculate at least one of the one or more buffer management parameters based on a buffer size.

46. The system of claim 43, wherein the one or more buffer management parameters comprise a watermark level.

47. The system of claim 46, wherein the watermark level comprises a lower bound of a desired watermark level range.

48. The system of claim 46, wherein the watermark level comprises an upper bound of a desired watermark level range.

49. The system of claim 43, wherein the one or more buffer management parameters comprise a burst length.

50. The system of claim 49, wherein the burst length comprises a lower bound of a desired burst length range.

51. The apparatus of claim 49, wherein the burst length comprises an upper bound of a desired burst length range.

52. The system of claim 43, wherein the data processor is further configured to detect a change from a first display mode to a second display mode, and in response to the detecting is further configured to calculate at least one of the one or more buffer management parameters based on the second display mode.

53. The system of claim 43, wherein the data processor is further configured to detect a change from a first system configuration to a second system configuration, and in response to the detecting is further configured to calculate at least one of the one or more buffer management parameters based on the second system configuration.

54. The system of claim 43, wherein the latency parameter represents a maximum expected latency time amount for the first system configuration.

55. The system of claim 43, wherein the first display mode is characterized by at least one of a first refresh rate, a first display resolution, and a first color depth.

56. The apparatus of claim 43, wherein the first system configuration is characterized at least by a first buffer memory type.

57. A method of determining buffer management information for a data processing system, comprising:

determining a maximum amount of time that access to a local memory to obtain data to supply a display FIFO buffer memory may be delayed;

determining a drain rate at which data is to be drained from the display FIFO buffer memory based on a display mode supported by a graphics processor;

calculating a watermark value based on at least the maximum amount of time and the drain rate; and

making the watermark value available for management of the display FIFO buffer memory.

58. The method of claim 57, wherein calculating the watermark value comprises multiplying the maximum amount of time and the drain rate.

59. The method of claim 58, wherein the watermark value further comprises subtracting the product of the maximum amount of time and the drain rate from the size of the display FIFO buffer memory.

60. A method of determining buffer management information for a data processing system, comprising:

determining a maximum amount of time that access to a local memory to obtain data to supply a display FIFO buffer memory may be delayed;

determining a drain rate at which data is to be drained from the display FIFO buffer memory based on a display mode supported by a graphics processor;

calculating a burst length value based on at least the maximum amount of time and the drain rate; and

making the burst length value available for management of the display FIFO buffer memory.

61. The method of claim 60, wherein:

λ_{min} comprises the product of the maximum amount of time and the drain rate;

Φ comprises the size of the display FIFO buffer memory;

δ comprises the drain rate; and

calculating the burst length value comprises performing the following operation:

$$\lambda_{min} \times \left(\frac{\varphi}{\varphi - \delta} \right) .$$

62. The method of claim 60, wherein calculating the burst length value comprises subtracting the result of the performed operation from the size of the display FIFO buffer memory.

Evidence Appendix

None.

Related Proceedings Appendix

None.